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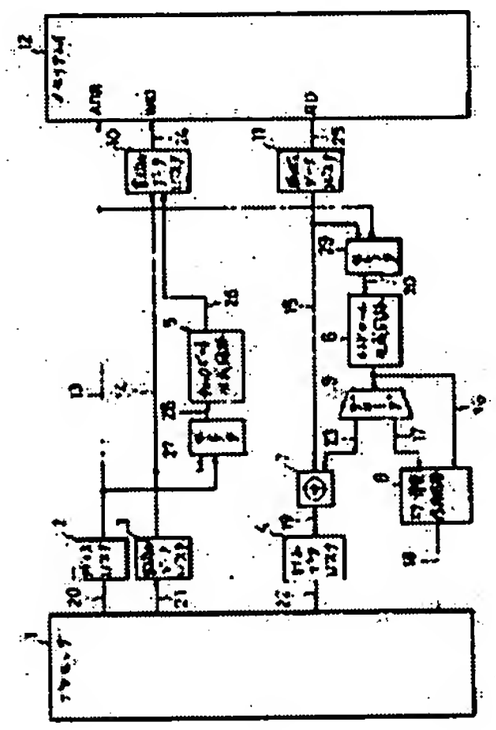
(72)Inventor : KUBOYA MAKOTO

(54) ADDRESS INCOINCIDENCE DETECTING CIRCUIT

(57)Abstract:
PURPOSE: To accurately detect the incoincidence of all data writing addresses with data reading addresses.
CONSTITUTION: At the time of writing data, address check bits for all bits of addresses are formed and written in a memory array 12. At the time of reading out data written in the array 12, address syndrome information is formed from all the bits of the addresses and the address check bits written in a storage element and coincidence/incoincidence between writing addresses and reading addresses is judged based upon the information.



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審査請求　未請求　請求項の数１(全　５　頁)

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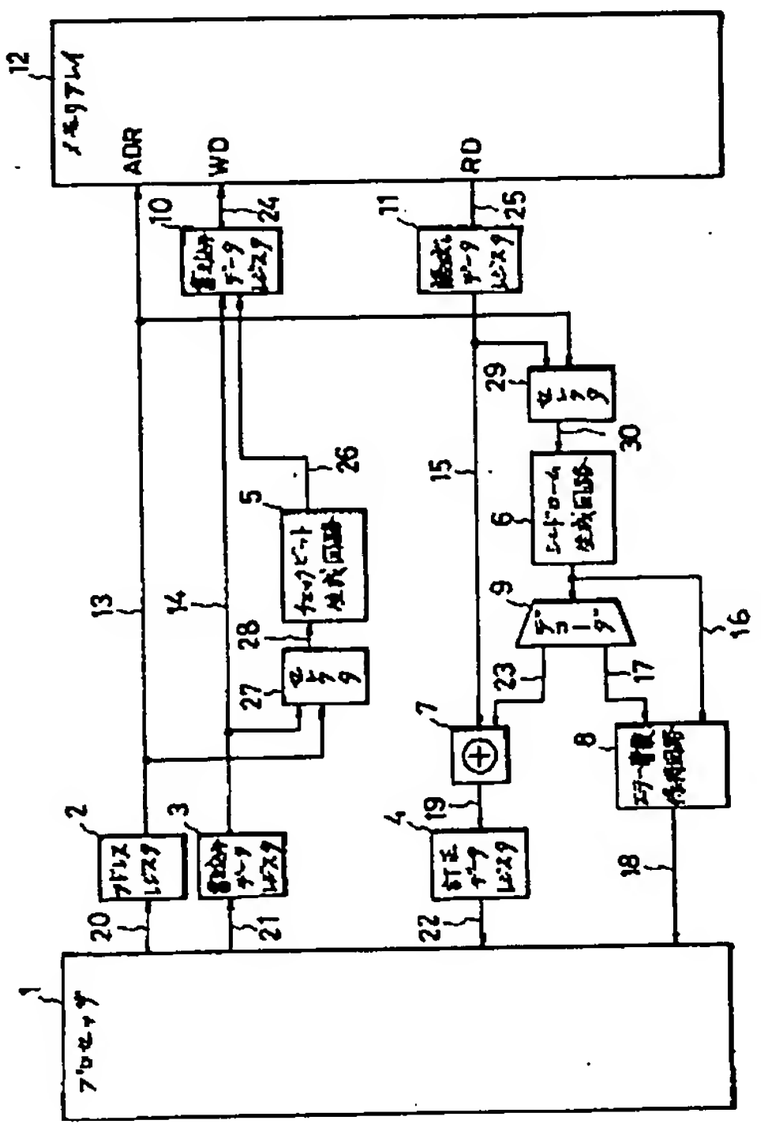
(54)【発明の名称】　アドレス不一致検出回路

(57)【要約】
【目的】　データ書き込み時のアドレスと読みだし時のアドレスとの不一致を全アドレスについて正確に検出できるようにする。
【構成】　データ書き込み時にはアドレスの全ビットについてアドレス用チェックビットが生成されメモリアレイ１２に書き込まれる。そしてメモリアレイ１２に書き込まれたデータの読みだし時にはアドレスの全ビットと記憶素子に書き込まれたアドレス用チェックビットとからアドレス用シンドローム情報が生成され、この情報に基づき書き込み時のアドレスと読みだし時のアドレスとの一致・不一致が判定される。



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【特許請求の範囲】
【請求項１】　主記憶装置に設けられデータの書き込みアドレスと読みだしアドレスとの不一致を検出するアドレス不一致検出回路おいて、
アドレスの全ビットからアドレス用チェックビットを生成すると共に記憶素子に書き込まれるデータの全ビットからデータ用チェックビットを生成して前記記憶素子へ書き込むチェックビット生成回路と、このチェックビット生成回路へのアドレス及びデータを選択する第１のセレクタと、アドレスの全ビットと記憶素子に書き込まれたアドレス用チェックビットとからアドレス用シンドローム情報を生成すると共に前記記憶素子からの読みだしデータと記憶素子に書き込まれたデータ用チェックビットとからデータ用シンドローム情報を生成するシンドローム生成回路と、前記アドレス用シンドローム情報を生成するためのアドレス及びアドレス用チェックビットと前記データ用シンドローム情報を生成するための前記読みだしデータ及びデータ用チェックビットとを選択して前記シンドローム生成回路へ与える第２のセレクタと、前記シンドローム生成回路から出力されたシンドローム情報を取り込んで書き込み時のアドレスと読みだし時のアドレスとの一致・不一致を検出するデコーダとを備えたことを特徴とするアドレス不一致検出回路。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、主記憶装置に設けられデータの書き込みアドレスと読みだしアドレスとの不一致を検出するアドレス不一致検出回路に関する。
【０００２】
【従来の技術】従来、この種のアドレス不一致検出回路は、アドレスの全ビットについて排他的論理和を行い１ビットのアドレスパリティビットを生成すると共に、データの書き込み時にはチェックビット生成回路にアドレスパリティビットを組み込んでチェックビットを生成し、このチェックビットを書き込みデータと共に記憶素子へ書き込みようにしている。そして、データの読みだし時には読みだしデータと同時にチェックビットも読みだすようにし、書き込み時のアドレスパリティビットと読みだし時のアドレスパリティビットとを比較しこれらの一致・不一致を判定するようにしている。
【０００３】
【発明が解決しようとする課題】従来のアドレス不一致検出回路は、アドレスの不一致を検出する場合、アドレスの全ビットについて排他的論理和演算を行いアドレスパリティビットを生成するようにしている。このため、例えばデータの書き込み時のアドレスと読みだし時のアドレスのうち任意の２ビットが反転して不一致となっているような場合にも、アドレスパリティビットの値は双方のアドレスが一致している場合と変わらないことから、双方のアドレスが一致と判定され、アドレスの不一致が正確に検出できないという問題があった。

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【０００４】
【課題を解決するための手段】このような課題を解決するために本発明は、アドレスの全ビットからアドレス用チェックビットを生成すると共に記憶素子に書き込まれるデータの全ビットからデータ用チェックビットを生成して記憶素子へ書き込むチェックビット生成回路と、このチェックビット生成回路へのアドレス及びデータを選択する第１のセレクタと、アドレスの全ビットと記憶素子に書き込まれたアドレス用チェックビットとからアドレス用シンドローム情報を生成すると共に記憶素子からの読みだしデータと記憶素子に書き込まれたデータ用チェックビットとからデータ用シンドローム情報を生成するシンドローム生成回路と、アドレス用シンドローム情報を生成するためのアドレス及びアドレス用チェックビットとデータ用シンドローム情報を生成するための読みだしデータ及びデータ用チェックビットとを選択してシンドローム生成回路へ与える第２のセレクタと、シンドローム生成回路から出力されたシンドローム情報を取り込んで書き込み時のアドレスと読みだし時のアドレスとの一致・不一致を検出するデコーダとを備えたものである。
【０００５】
【作用】データ書き込み時にはアドレスの全ビットについてアドレス用チェックビットが生成され記憶素子に書き込まれる。そして記憶素子に書き込まれたデータの読みだし時にはアドレスの全ビットと記憶素子に書き込まれたアドレス用チェックビットとからアドレス用シンドローム情報が生成され、この情報に基づき書き込み時のアドレスと読みだし時のアドレスとの一致・不一致が判定される。
【０００６】
【実施例】以下、本発明について図面を参照して説明する。図１は、本発明に係るアドレス不一致検出回路の一実施例を示すブロック図である。同図において、プロセッサ１からのアドレス出力は、アドレス線２０を介してアドレスレジスタ２へ接続され、アドレスレジスタ２は、アドレス線１３を介しセレクタ２７，２９及びメモリアレイ１２のアドレス端子（以下、ＡＤＲ端子）と接続されている。また、プロセッサ１からのデータ出力は、書き込みデータ線２１を介して書き込みデータレジスタ３へ送出され、書き込みデータレジスタ３は、書き込みデータ線１４を介してセレクタ２７及び書き込みデータレジスタ１０に接続されている。また、セレクタ２７は、アドレスまたは書き込みデータにそれぞれ固有の符号であるチェックビットを生成するチェックビット生成回路５とアドレスデータ線２８を介して接続されている。
【０００７】書き込みデータレジスタ１０は、入力側には書き込みデータレジスタ３の出力とチェックビット生

成回路５の出力とが接続されると共に、出力側は記憶素子書き込みデータ線２４を介してメモリアレイ１２の書き込みデータ端子（以下、ＷＤ端子）と接続されている。また、メモリアレイ１２からのデータ出力は、読みだしデータ端子（以下、ＲＤ端子），読みだしデータ線２５を介して読みだしデータレジスタ１１へ接続される。ここで、読みだしデータレジスタ１１は読みだしデータ線１５を介してセレクタ２９及び誤りビット訂正回路７に接続されている。また、セレクタ２９はアドレスデータ線３０を介し、アドレスまたは読みだしデータ及びそれぞれ固有のチェックビットの誤りの有無を判別する符号であるシンドローム情報を生成するシンドローム生成回路６と接続されている。

【０００８】シンドローム生成回路６の出力は、シンドローム情報信号線１６を介してエラー情報保持回路８及び取り込んだシンドローム情報が「０」か否かでエラーの発生の有無を判断するデコーダ９に接続され、さらにデコーダ９はそれぞれ誤りビット位置情報信号線２３及びエラー情報信号線１７を介し誤りビット訂正回路７及びエラー情報保持回路８に接続されている。さらに、誤りビット訂正回路７の出力は、読みだしデータ線１９を介して訂正データレジスタ４へ送出されると共に、訂正データレジスタ４は訂正データ線２２を介してプロセッサ１と接続されている。また、エラー情報保持回路８の出力は、エラー報告信号線１８を介してプロセッサ１へ接続される。

【０００９】次に、このアドレス不一致検出回路の動作について説明する。はじめに書き込み時の動作から説明する。プロセッサ１から出力されたアドレス信号は、アドレスレジスタ２を経てセレクタ２７とメモリアレイ１２のＡＤＲ端子へ出力される。セレクタ２７は、アドレス信号を選択しチェックビット生成回路５へ出力する。チェックビット生成回路５は、アドレス信号を受け取ってアドレス用のチェックビットを生成し、書き込みデータレジスタ１０へ出力する。

【００１０】一方、プロセッサ１から出力された書き込みデータは、書き込みデータレジスタ３を経て書き込みデータレジスタ１０とセレクタ２７とに出力される。セレクタ２７は、書き込みデータ線１４に出力される書き込みデータを選択しチェックビット生成回路５へ出力する。チェックビット生成回路５は、書き込みデータを受け取ってデータ用のチェックビットを生成し書き込みデータレジスタ１０へ出力する。書き込みデータ，データ用チェックビット，アドレス用チェックビットは、書き込みデータレジスタ１０からメモリアレイ１２のＷＤ端子へ出力され記憶素子に書き込まれる。

【００１１】次に、読みだし時の動作について説明する。プロセッサ１から出力されたアドレス信号は、アドレスレジスタ２を経てセレクタ２９とメモリアレイ１２のＡＤＲ端子に出力される。出力されたアドレスに書き

込まれている読みだしデータ，データ用チェックビット，アドレス用チェックビットは、メモリアレイ１２のＲＤ端子，読みだしデータレジスタ１１を経てセレクタ２９へ出力される。セレクタ２９は、アドレス信号とメモリアレイ１２から出力されたアドレス用チェックビットを選択してシンドローム生成回路６へ出力する。シンドローム生成回路６はアドレス信号とアドレス用チェックビット信号とを取り込みアドレス用のシンドローム情報を生成する。

【００１２】シンドローム生成回路６は、生成したシンドローム情報をデコーダ９とエラー情報保持回路８とへ出力する。デコーダ９は受け取ったシンドローム情報が「０」ではないときには、書き込み時のアドレスと読みだし時のアドレスとが一致していないと判断し、エラー情報信号線１７へアドレス不一致エラー信号を出力する。エラー情報保持回路８は、デコーダ９から出力されたアドレス不一致エラー信号を取り込み、エラー報告信号線１８を介しプロセッサ１へアドレス不一致エラーの報告を行う。

【００１３】また、デコーダ９は、受け取ったシンドローム情報が「０」ならば、書き込み時のアドレスと読みだし時のアドレスとが一致していると判断し、この場合セレクタ２９は読みだしデータとデータ用チェックビットとを選択してシンドローム生成回路６へ送出する。シンドローム生成回路６は、読みだしデータとデータチェック用ビットとを取り込み、シンドローム情報を生成しデコーダ９とエラー情報保持回路８とに送出する。

【００１４】この場合、デコーダ９は生成されたシンドローム情報からエラー無しか訂正可能なエラーか、或いは訂正不可能なエラーかを判断し、訂正可能なエラーならば誤りビット位置情報信号線２３を介し誤りビット位置情報信号をビット訂正回路７へ出力して訂正を行わせ、この結果を訂正データレジスタ４を介しプロセッサ１へ送出させる。一方、デコーダ９が訂正不可能エラーと判断した場合は、訂正不可能エラー情報信号をエラー情報保持回路８へ出力する。そして、エラー情報保持回路８は、プロセッサ１に訂正不可能エラーの報告を行う。

【００１５】このように、チェックビット生成回路５は、アドレスの全ビットに亙ってアドレス用チェックビットを生成し、これを書き込みデータと共に記憶素子に書き込む。そして読みだし時にシンドローム生成回路６は、アドレスの全ビットと記憶素子に書き込まれたアドレス用チェックビットとからアドレス用シンドローム情報を生成しデコーダ９へ出力する。デコーダ９は、シンドローム情報を取り込み、書き込み時のアドレスと読みだし時のアドレスとが一致しているか否かを判断し、不一致の場合にはアドレス不一致エラーを出力することにより、全アドレスに亙って書き込みアドレスと読みだしアドレスとの不一致が正確に検出でき、アドレス系回路

の信頼性を向上させることが可能となる。

【0016】

【発明の効果】以上説明したように本発明は、データ書き込み時にはアドレスの全ビットについてアドレス用チェックビットを生成してこれを記憶素子に書き込むと共に、データ読みだし時にはアドレスの全ビットと記憶素子に書き込まれたアドレス用チェックビットとからアドレス用シンドローム情報を生成して、この情報に基づき書き込み時のアドレスと読みだし時のアドレスとの一致・不一致を判定するようにしたので、書き込みアドレスと読みだしアドレスとの不一致が全アドレスについて正確に検出できるという効果がある。

【図面の簡単な説明】

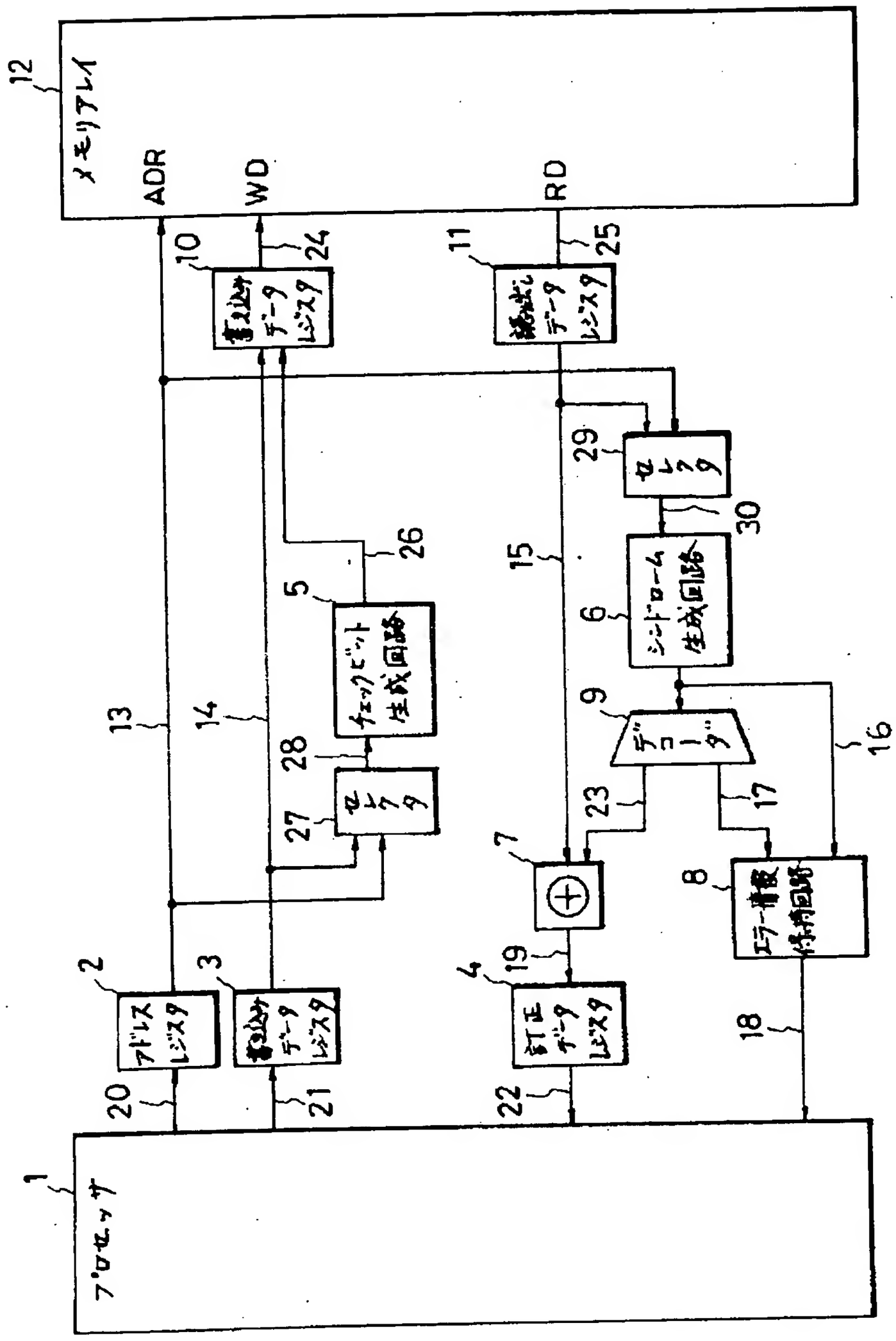
【図1】本発明に係るアドレス不一致検出回路の一実施

例を示すブロック図である。

【符号の説明】

1	プロセッサ
2	アドレスレジスタ
3，10	書き込みレジスタ
4	訂正データレジスタ
5	チェックビット生成回路
6	シンドローム生成回路
7	誤りビット訂正回路
8	エラー情報保持回路
9	デコーダ
11	読みだしデータレジスタ
12	メモリアレイ

【図1】


12
メモリアレイ
ADR
WD
RD
10
24
11
25
書込みデータレジスタ
読出しデータレジスタ
29
セレクタ
30
シンドローム生成回路
6
15
5
26
チェックビット生成回路
13
14
28
27
セレクタ
9
デコーダ
16
23
17
7
8
エラー情報保持回路
2
3
アドレスレジスタ
書込みデータレジスタ
4
19
訂正データレジスタ
18
20
21
22
1
アドレス

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CLAIMS

[Claim(s)]
[Claim 1] It is. the address inequality detector which is established in main storage, reads with the write-in address of data, and detects an inequality with the address -- The check bit generation circuit which generates the check bit for data from all the bits of the data written in a storage element while generating the check bit for the addresses from all the bits of the address, and is written in said storage element, The 1st selector which chooses the address and data to this check bit generation circuit, While generating the syndrome information for the addresses from all the bits of the address, and the check bit for the addresses written in the storage element The syndrome generation circuit which generates the syndrome information for data from the check bit for data written in readout data and a storage element from said storage element, The 2nd selector which chooses said readout data and the check bit for data for generating the address for generating said syndrome information for the addresses and the check bit for the addresses, and said syndrome information for data, and is given to said syndrome generation circuit, The address inequality detector characterized by having the decoder which incorporates and writes in the outputted syndrome information from said syndrome generation circuit, reads with the address at the time, and detects coincidence and an inequality with the address at the time.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the address inequality detector which is established in main storage, reads with the write-in address of data, and detects an inequality with the address.

[0002]
[Description of the Prior Art] Conventionally, this kind of address inequality detector includes an address parity bit in a check bit generation circuit at the time of the writing of data, generates a check bit, writes in this check bit, and with data, it is written in a storage element and it makes it like while it performs an exclusive OR about all the bits of the address and generates a 1-bit address parity bit. And it reads at the time of the readout of data, a check bit is also read to data and coincidence, it reads with the address parity bit at the time of writing, and he measures the address parity bit at the time, and is trying to judge these coincidence and inequalities.
[0003]
[Problem(s) to be Solved by the Invention] When detecting the inequality of the address, the conventional address inequality detector performs EXCLUSIVE OR operation about all the bits of the address, and he is trying to generate an address parity bit. for this reason -- for example, also when it read with the address at the time of the writing of data, 2 bits of arbitration of the address at the time were reversed and it had become an inequality, since the value of an address parity bit was not different from the case where both addresses are in agreement, both addresses were judged to be coincidence and it had the problem that the inequality of the address could not detect correctly.
[0004]
[Means for Solving the Problem] The check bit generation circuit which generates the check bit for data from all the bits of the data written in a storage element while this invention generates the check bit for the addresses from all the bits of the address, in order to solve such a technical problem, and is written in a storage element, The 1st selector which chooses the address and data to this check bit generation circuit, While generating the syndrome information for the addresses from all the bits of the address, and the check bit for the addresses written in the storage element The syndrome generation circuit which generates the syndrome information for data from the check bit for data written in readout data and a storage element from the storage element, The 2nd selector which chooses the check bit for readout data and data for generating the address for generating the syndrome information for the addresses and the check bit for the addresses, and the syndrome information for data, and is given to a syndrome generation circuit, It has the decoder which incorporates and writes in the outputted syndrome information from a syndrome generation circuit, reads with the address at the time, and detects coincidence and an inequality with the address at the time.
[0005]
[Function] At the time of data writing, the check bit for the addresses is generated about all the bits of the address, and it is written in a storage element. And at the time of the readout of the data written in the storage element, the syndrome information for the addresses is generated from all the bits of the address, and the check bit for the addresses written in the storage element, it reads with the address at the time of writing based on this information, and coincidence and an inequality with the address at the time are judged.
[0006]
[Example] Hereafter, this invention is explained with reference to a drawing. Drawing 1 is the block diagram showing one example of the address inequality detector concerning this invention. In this drawing, the address output from a processor 1 is connected to an

address register 2 through the address line 20, and the address register 2 is connected with the address terminal (henceforth, ADR terminal) of selectors 27 and 29 and a memory array 12 through the address line 13. Moreover, the data output from a processor 1 is written in through the write-in data line 21, and is sent out to a data register 3, and the write-in data register 3 is connected to the selector 27 and the write-in data register 10 through the write-in data line 14. Moreover, the selector 27 is connected to the address or write-in data through the check bit generation circuit 5 and the address-data line 28 which generate the check bit which is the sign of a proper, respectively.

[0007] While writing the write-in data register 10 in an input side and connecting the output of a data register 3, and the output of the check bit generation circuit 5, the output side is connected with the write-in data terminal (henceforth, WD terminal) of a memory array 12 through the storage element write-in data line 24. Moreover, the data output from a memory array 12 is read through a readout data terminal (henceforth, RD terminal) and the readout data line 25, and is connected to a data register 11. Here, the readout data register 11 is connected to the selector 29 and the error bit correction circuit 7 through the readout data line 15. Moreover, the selector 29 is connected with the syndrome generation circuit 6 which generates the syndrome information which is the address or readout data, and the sign that distinguishes the existence of the error of the check bit of a proper, respectively through the address-data line 30.

[0008] The output of the syndrome generation circuit 6 is connected to the decoder 9 which judges the existence of generating of the error of the error information holding circuit 8 and the incorporated syndrome information by whether it is "0" through the syndrome information signal line 16, and the decoder 9 is further connected to the error bit correction circuit 7 and the error information holding circuit 8 through the error bit-position information signal line 23 and the error information signal line 17, respectively. Furthermore, while the output of the error bit correction circuit 7 is sent out through the readout data line 19 to the correction data register 4, the correction data register 4 is connected with the processor 1 through the correction data line 22. Moreover, the output of the error information holding circuit 8 is connected to a processor 1 through the error report signal line 18.

[0009] Next, actuation of this address inequality detector is explained. It writes in first and explains from the actuation at the time. The address signal outputted from the processor 1 is outputted to the ADR terminal of a selector 27 and a memory array 12 through an address register 2. A selector 27 chooses an address signal and outputs it to the check bit generation circuit 5. The check bit generation circuit 5 receives an address signal, generates the check bit for the addresses, and outputs it to the write-in data register 10.

[0010] On the other hand, the write-in data outputted from the processor 1 are written in through the write-in data register 3, and are outputted to a data register 10 and a selector 27. A selector 27 chooses the write-in data outputted to the write-in data line 14, and outputs them to the check bit generation circuit 5. The check bit generation circuit 5 receives write-in data, generates the check bit for data, and outputs it to the write-in data register 10. The check bit for write-in data and data and the check bit for the addresses are outputted to WD terminal of a memory array 12 from the write-in data register 10, and are written in a storage element.

[0011] Next, the actuation at the time of a readout is explained. The address signal

outputted from the processor 1 is outputted to the ADR terminal of a selector 29 and a memory array 12 through an address register 2. The readout data currently written in the outputted address, the check bit for data, and the check bit for the addresses are outputted to a selector 29 through RD terminal of a memory array 12, and the readout data register 11. A selector 29 chooses the check bit for the addresses outputted from the address signal and the memory array 12, and outputs it to the syndrome generation circuit 6. The syndrome generation circuit 6 incorporates an address signal and the check bit signal for the addresses, and generates the syndrome information for the addresses.

[0012] The syndrome generation circuit 6 outputs the generated syndrome information to a decoder 9 and the error information holding circuit 8. When the received syndrome information is not "0", a decoder 9 reads with the address at the time of writing, judges that the address at the time is not in agreement, and outputs an address inequality error signal to the error information signal line 17. The error information holding circuit 8 incorporates the address inequality error signal outputted from the decoder 9, and reports an address inequality error to a processor 1 through the error report signal line 18.

[0013] Moreover, if the received syndrome information "0" Becomes, a decoder 9 reads with the address at the time of writing, and it judges that the address at the time is in agreement, and in this case, a selector 29 chooses readout data and the check bit for data, and it sends it out to the syndrome generation circuit 6. The syndrome generation circuit 6 incorporates readout data and the bit for data check, generates syndrome information, and sends it out to a decoder 9 and the error information holding circuit 8.

[0014] in this case, the error whose decoder 9 can correct only nothing [error] from the generated syndrome information -- or the error which cannot be corrected is judged, if it is the error which can be corrected, it will be made to correct by outputting an error bit-position information signal to the bit correction circuit 7 through the error bit-position information signal line 23, and this result will be sent out to a processor 1 through the correction data register 4. On the other hand, when a decoder 9 judges it as a correction impossible error, a correction impossible error information signal is outputted to the error information holding circuit 8. And the error information holding circuit 8 reports a correction impossible error to a processor 1.

[0015] Thus, the check bit generation circuit 5 extends for all the bits of the address, generates the check bit for the addresses, writes this in, and writes it in a storage element with data. And at the time of a readout, the syndrome generation circuit 6 generates the syndrome information for the addresses from all the bits of the address, and the check bit for the addresses written in the storage element, and outputs it to a decoder 9. By judging whether a decoder 9 incorporates syndrome information, and reads with the address at the time of writing, and its address at the time corresponds, and outputting an address inequality error in the case of an inequality, it continues and writes in all the addresses and reads with the address, and an inequality with the address can detect correctly and it becomes possible to raise address system circuit reliability of it.

[0016]

[Effect of the Invention] As explained above, while this invention generates the check bit for the addresses about all the bits of the address at the time of data writing and writing this in a storage element At the time of a data readout, the syndrome information for the addresses is generated from all the bits of the address, and the check bit for the addresses written in the storage element. Since it reads with the address at the time of writing based

on this information and coincidence and an inequality with the address at the time were judged, it reads with the write-in address and is effective in the ability of an inequality with the address to detect correctly about all the addresses.

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TECHNICAL FIELD

[Industrial Application] This invention relates to the address inequality detector which is established in main storage, reads with the write-in address of data, and detects an inequality with the address.

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PRIOR ART

[Description of the Prior Art] Conventionally, this kind of address inequality detector includes an address parity bit in a check bit generation circuit at the time of the writing of data, generates a check bit, writes in this check bit, and with data, it is written in a storage element and it makes it like while it performs an exclusive OR about all the bits of the address and generates a 1-bit address parity bit. And it reads at the time of the readout of data, a check bit is also read to data and coincidence, it reads with the address parity bit at the time of writing, and he measures the address parity bit at the time, and is trying to judge these coincidence and inequalities.

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EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, while this invention generates the check bit for the addresses about all the bits of the address at the time of data writing and writing this in a storage element At the time of a data readout, the syndrome information for the addresses is generated from all the bits of the address, and the check bit for the addresses written in the storage element. Since it reads with the address at the time of writing based on this information and coincidence and an inequality with the address at the time were judged, it reads with the write-in address and is effective in the ability of an inequality with the address to detect correctly about all the addresses.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] When detecting the inequality of the address, the conventional address inequality detector performs EXCLUSIVE OR operation about all the bits of the address, and he is trying to generate an address parity bit. for this reason -- for example, also when it read with the address at the time of the writing of data, 2 bits of arbitration of the address at the time were reversed and it had become an inequality, since the value of an address parity bit was not different from the case where both addresses are in agreement, both addresses were judged to be coincidence and it had the problem that the inequality of the address could not detect correctly.

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MEANS

[Means for Solving the Problem] The check bit generation circuit which generates the check bit for data from all the bits of the data written in a storage element while this invention generates the check bit for the addresses from all the bits of the address, in order to solve such a technical problem, and is written in a storage element, The 1st selector which chooses the address and data to this check bit generation circuit, While generating the syndrome information for the addresses from all the bits of the address, and the check bit for the addresses written in the storage element The syndrome generation circuit which generates the syndrome information for data from the check bit for data written in readout data and a storage element from the storage element, The 2nd selector which chooses the check bit for readout data and data for generating the address for generating the syndrome information for the addresses and the check bit for the addresses, and the syndrome information for data, and is given to a syndrome generation circuit, It has the decoder which incorporates and writes in the outputted syndrome information from a syndrome generation circuit, reads with the address at the time, and detects coincidence and an inequality with the address at the time.

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OPERATION

[Function] At the time of data writing, the check bit for the addresses is generated about all the bits of the address, and it is written in a storage element. And at the time of the readout of the data written in the storage element, the syndrome information for the addresses is generated from all the bits of the address, and the check bit for the addresses written in the storage element, it reads with the address at the time of writing based on this information, and coincidence and an inequality with the address at the time are judged.

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EXAMPLE

[Example] Hereafter, this invention is explained with reference to a drawing. Drawing 1 is the block diagram showing one example of the address inequality detector concerning this invention. In this drawing, the address output from a processor 1 is connected to an address register 2 through the address line 20, and the address register 2 is connected with the address terminal (henceforth, ADR terminal) of selectors 27 and 29 and a memory array 12 through the address line 13. Moreover, the data output from a processor 1 is written in through the write-in data line 21, and is sent out to a data register 3, and the write-in data register 3 is connected to the selector 27 and the write-in data register 10 through the write-in data line 14. Moreover, the selector 27 is connected to the address or write-in data through the check bit generation circuit 5 and the address-data line 28 which generate the check bit which is the sign of a proper, respectively.

[0007] While writing the write-in data register 10 in an input side and connecting the output of a data register 3, and the output of the check bit generation circuit 5, the output side is connected with the write-in data terminal (henceforth, WD terminal) of a memory array 12 through the storage element write-in data line 24. Moreover, the data output from a memory array 12 is read through a readout data terminal (henceforth, RD terminal) and the readout data line 25, and is connected to a data register 11. Here, the readout data register 11 is connected to the selector 29 and the error bit correction circuit 7 through the readout data line 15. Moreover, the selector 29 is connected with the syndrome generation circuit 6 which generates the syndrome information which is the address or readout data, and the sign that distinguishes the existence of the error of the check bit of a proper, respectively through the address-data line 30.

[0008] The output of the syndrome generation circuit 6 is connected to the decoder 9 which judges the existence of generating of the error of the error information holding circuit 8 and the incorporated syndrome information by whether it is "0" through the syndrome information signal line 16, and the decoder 9 is further connected to the error bit correction circuit 7 and the error information holding circuit 8 through the error bit-position information signal line 23 and the error information signal line 17, respectively. Furthermore, while the output of the error bit correction circuit 7 is sent out through the readout data line 19 to the correction data register 4, the correction data register 4 is connected with the processor 1 through the correction data line 22. Moreover, the output of the error information holding circuit 8 is connected to a processor 1 through the error report signal line 18.

[0009] Next, actuation of this address inequality detector is explained. It writes in first and explains from the actuation at the time. The address signal outputted from the processor 1 is outputted to the ADR terminal of a selector 27 and a memory array 12 through an address register 2. A selector 27 chooses an address signal and outputs it to the check bit generation circuit 5. The check bit generation circuit 5 receives an address signal, generates the check bit for the addresses, and outputs it to the write-in data register 10.

[0010] On the other hand, the write-in data outputted from the processor 1 are written in through the write-in data register 3, and are outputted to a data register 10 and a selector 27. A selector 27 chooses the write-in data outputted to the write-in data line 14, and outputs them to the check bit generation circuit 5. The check bit generation circuit 5 receives write-in data, generates the check bit for data, and outputs it to the write-in data register 10. The check bit for write-in data and data and the check bit for the addresses

are outputted to WD terminal of a memory array 12 from the write-in data register 10, and are written in a storage element.

[0011] Next, the actuation at the time of a readout is explained. The address signal outputted from the processor 1 is outputted to the ADR terminal of a selector 29 and a memory array 12 through an address register 2. The readout data currently written in the outputted address, the check bit for data, and the check bit for the addresses are outputted to a selector 29 through RD terminal of a memory array 12, and the readout data register 11. A selector 29 chooses the check bit for the addresses outputted from the address signal and the memory array 12, and outputs it to the syndrome generation circuit 6. The syndrome generation circuit 6 incorporates an address signal and the check bit signal for the addresses, and generates the syndrome information for the addresses.

[0012] The syndrome generation circuit 6 outputs the generated syndrome information to a decoder 9 and the error information holding circuit 8. When the received syndrome information is not "0", a decoder 9 reads with the address at the time of writing, judges that the address at the time is not in agreement, and outputs an address inequality error signal to the error information signal line 17. The error information holding circuit 8 incorporates the address inequality error signal outputted from the decoder 9, and reports an address inequality error to a processor 1 through the error report signal line 18.

[0013] Moreover, if the received syndrome information "0" Becomes, a decoder 9 reads with the address at the time of writing, and it judges that the address at the time is in agreement, and in this case, a selector 29 chooses readout data and the check bit for data, and it sends it out to the syndrome generation circuit 6. The syndrome generation circuit 6 incorporates readout data and the bit for data check, generates syndrome information, and sends it out to a decoder 9 and the error information holding circuit 8.

[0014] in this case, the error whose decoder 9 can correct only nothing [error] from the generated syndrome information -- or the error which cannot be corrected is judged, if it is the error which can be corrected, it will be made to correct by outputting an error bit-position information signal to the bit correction circuit 7 through the error bit-position information signal line 23, and this result will be sent out to a processor 1 through the correction data register 4. On the other hand, when a decoder 9 judges it as a correction impossible error, a correction impossible error information signal is outputted to the error information holding circuit 8. And the error information holding circuit 8 reports a correction impossible error to a processor 1.

[0015] Thus, the check bit generation circuit 5 extends for all the bits of the address, generates the check bit for the addresses, writes this in, and writes it in a storage element with data. And at the time of a readout, the syndrome generation circuit 6 generates the syndrome information for the addresses from all the bits of the address, and the check bit for the addresses written in the storage element, and outputs it to a decoder 9. By judging whether a decoder 9 incorporates syndrome information, and reads with the address at the time of writing, and its address at the time corresponds, and outputting an address inequality error in the case of an inequality, it continues and writes in all the addresses and reads with the address, and an inequality with the address can detect correctly and it becomes possible to raise address system circuit reliability of it.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing one example of the address inequality detector concerning this invention.

[Description of Notations]
1 Processor
2 Address Register
3 Ten Write-in register
4 Correction Data Register
5 Check Bit Generation Circuit
6 Syndrome Generation Circuit
7 Error Bit Correction Circuit
8 Error Information Holding Circuit
9 Decoder
11 Readout Data Register
12 Memory Array